# DSP Development Kit

# Getting Started User Guide

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P25-36388-00

Document Version: 1.0
Document Date: October 2008

UG-01052-1.0

# Contents

# 1. About This Kit

## Introduction

Welcome to the Altera® DSP Development Kit. This kit provides a platform for experimenting with Digital Signal Processing (DSP) using Altera's design environment and intellectual property. Included are a Data Conversion system containing a full-featured FPGA development platform, hardware and software development tools, documentation, and accessories needed to begin DSP development.

## Kit Features

Kit contents vary depending on which DSP development platform you have purchased.

### DSP Development Kit, Stratix III Edition

The DSP Development Kit, Stratix® III Edition contains:

- **A Stratix III Development Board**—a hardware platform with integrated USB-Blaster™ and EP3SL150 FPGA to support the Data Conversion High-Speed Mezzanine Card (HSMC). The board also provides power for the Data Conversion HSMC.

  For information about setting up and powering up the Stratix III development board, refer to the *Stratix III Development Kit User Guide.* For detailed information about the components and interfaces included on the Stratix III development board, and about their locations on the board, refer to the *Stratix III Development Board Reference Manual*.

- **A Data Conversion HSMC**—a prototyping platform that allows you to develop high-performance DSP designs. Key features of the Data Conversion HSMC include two high-speed analog-to-digital (A/D) converters, a dual digital-to-analog (D/A) converter, and a Stereo Audio coder/decoder (CODEC).

  For detailed information about the components and interfaces included on the Data Conversion HSMC, and about their locations on the board, refer to the *Data Conversion HSMC Reference Manual*.

- **DSP Development Kit, Stratix III Edition CD-ROM**—This CD-ROM includes several designs for exercising the Data Conversion HSMC. In addition, the following items are included:
  - Reference designs for DSP application
  - Design examples
  - *Data Conversion HSMC Reference Manual*
  - *Stratix III Development Board Reference Manual*
  - *DSP Development Kit Getting Started User Guide* (this document)
  - Device data sheets and tutorials
  - Schematic and board design files
- **Altera Complete Design Suite DVD**—This DVD includes the following items:
  - Quartus® II Software, Development Kit Edition (DKE)—The Quartus II software integrates in nearly any design environment, with interfaces to industry-standard electronic design automation (EDA) tools.

    The Quartus II DKE software license allows you to use the product for 12 months. After 12 months, you must purchase a renewal subscription to continue using the software. For more information, refer to the Altera website at www.altera.com.

  - MegaCore® IP Library
  - Nios® II Embedded Design Suite
  - ModelSim®—Altera Edition
  - DSP Builder
- **MathWorks MATLAB/Simulink CD-ROM**—This CD-ROM contains third-party tools that are used in conjunction with DSP Builder as part of Altera's DSP development flow. MATLAB is a high-level technical computing language environment for algorithm development, data visualization, data analysis, and numerical computation. Simulink provides an interactive graphical environment and a customizable set of block libraries that let you accurately design, simulate, implement, and test signal processing systems.

  A 30-day license for MATLAB/Simulink software is included as part of the DSP development kit. To obtain the personal license password and for more information, visit MathWorks at www.mathworks.com.

## DSP Development Kit, Cyclone III Edition

The DSP Development Kit, Cyclone® III Edition contains:

- **A Cyclone III Development Board**—a hardware platform with integrated USB-Blaster and EP3C120 FPGA to support the Data Conversion HSMC. The board also provides power for the Data Conversion HSMC.

  For information about setting up and powering up the Cyclone III development board, refer to the *Cyclone III Development Kit User Guide*. For detailed information about the components and interfaces included on the Cyclone III development board, and about their locations on the board, refer to the *Cyclone III Development Board Reference Manual*.

- **A Data Conversion HSMC**—refer to "DSP Development Kit, Stratix III Edition" on page 1–1 for more information.
- **DSP Development Kit, Cyclone III Edition CD-ROM**—This CD-ROM includes the following items:
  - Reference designs for DSP application
  - Design examples
  - *Data Conversion HSMC Reference Manual*
  - *Cyclone III Development Board Reference Manual*
  - *DSP Development Kit Getting Started User Guide* (this document)
  - Device data sheets and tutorials
  - Schematic and board design files
- **Altera Complete Design Suite DVD**—This DVD includes the following items:
  - Free Quartus II Web Edition software license, Windows platform only

    For more information, refer to the Altera website at *www.altera.com/products/software/products/quartus2web/sof-quarwebmain.html*.

  - MegaCore IP Library
  - Nios II Embedded Design Suite
  - ModelSim—Altera Web Edition
  - DSP Builder
- **MathWorks MATLAB/Simulink CD-ROM**—refer to "DSP Development Kit, Stratix III Edition" on page 1–1 for information about the CD-ROM contents.

## DSP Development Kit, Stratix II EP2S60 and EP2S180 Editions

The DSP Development Kit, Stratix II Edition contains:

- **A Stratix II DSP Development Board (EP2S60 or EP2S180)**—a prototyping platform that allows you to develop high-performance DSP designs. Key features of the board include a Stratix II device, high-speed A/D and D/A converters, and connectors for Texas Instruments and Analog Devices evaluation boards.

  For specific information about the components and interfaces included on the board, refer to the *Stratix II DSP Development Board Data Sheet*.

- **DSP Development Kit, Stratix II Edition CD-ROM**—This CD-ROM includes the following items:
  - Reference designs for DSP application
  - Design examples
  - *Stratix II DSP Development Board Data Sheet*
  - *DSP Development Kit Getting Started User Guide* (this document)
  - Device data sheets and tutorials
  - Schematic and board design files
- **Altera Complete Design Suite DVD**—refer to "DSP Development Kit, Stratix III Edition" on page 1–1 for information about the DVD contents.
- **MathWorks MATLAB/Simulink CD-ROM**—refer to "DSP Development Kit, Stratix III Edition" on page 1–1 for information about the CD-ROM contents.

## Power Supply and Cable

The following items are included in all DSP development kits:

- USB-Blaster download cable

  The Stratix II kit contains a USB-Blaster for downloading designs, while the Stratix III and Cyclone III kits have USB-Blasters integrated on the development boards.

- SLP-50 anti-aliasing filter from Mini-Circuits
- Two SMA cables for interconnecting the devices on board
- USB cable for downloading designs
- CAT-5/RJ-45 cable
- Power supply and adapters for North America, Japan, Europe, and the United Kingdom

# 2. Getting Started

## Introduction

This user guide familiarizes you with the contents of the kit and guides you through the DSP development kit setup. Using this guide, you can do the following:

- Inspect the contents of the kit
- Install the Altera Complete Design Suite DVD
- Set up licensing
- Install the DSP Development Kit CD-ROM
- Set up, power up, and verify correct operation of the kit hardware
- Configure the FPGA
- Find and use the tutorials
- Set up and run included application examples and demonstrations

For complete details about the development board, refer to the development reference manual for your kit. If you have a system that uses a Data Conversion HSMC, refer to the *Data Conversion HSMC Reference Manual*.

## Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in this section. If any of the items are missing, contact Altera before you proceed.

### Check the Kit Contents

Refer to "Kit Features" on page 1–1 for the contents of your DSP development kit.

### Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

CAUTION

Without proper anti-static handling, the development board can be damaged.

Verify that all components are on the board and appear intact.

In typical applications with the development board, a heatsink is not necessary. However, under extreme conditions the board may require additional cooling to stay within operating temperature guidelines. You may wish to perform power consumption and thermal modeling to determine whether your application requires additional cooling.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

## Hardware Requirements

The Quartus II software has some minimum system requirements. Otherwise, the DSP development kit provides all of the hardware needed to use the board.

For Quartus II requirements, refer to the *Quartus II Installation & Licensing for Windows Manual*.

## Software Requirements

The development kit requires the following software:

- Windows XP operating system.
- Quartus II software.
- MathWorks MATLAB and Simulink DSP system design and modeling tools provided on the MathWorks MATLAB/Simulink CD-ROM. This software is required to create hardware description language (HDL) designs that use blocks from DSP Builder.

Refer to the *Quartus II Installation & Licensing for Windows Manual* for more information about the Quartus II system software requirements, especially heeding the following:

- A web browser, Microsoft Internet Explorer version 5.0 or later or Firefox version 2.0 or later. You must have a web browser to register the Quartus II software and request license files. Refer to "Licensing Considerations" on page 3–4.
- Version 2.0 or later of the .NET framework.

If you receive an `Application Error` message when launching the demo application, install version 2.0 or later versions of the .NET framework. Some Windows versions do not have runtime DLL for the .NET application. The .NET framework application can be downloaded from the following location: www.microsoft.com/download.

# References

For other related information, refer to the following websites:

- For additional HSMCs available for purchase: www.altera.com/products/devkits/kit-daughter_boards.jsp
- For the Stratix III device documentation: www.altera.com/literature/lit-stx3.jsp
- For the Cyclone III device documentation: www.altera.com/literature/lit-cyc3.jsp

- For the Stratix II device documentation:
  www.altera.com/literature/lit-stx2.jsp
- For the Stratix III reference designs:
  www.altera.com/support/refdesigns/device/stratix3/stratix3-index.jsp
- For the Cyclone III reference designs:
  www.altera.com/support/refdesigns/device/cyclone3/cyclone3-index.jsp
- For the Stratix II reference designs:
  www.altera.com/support/refdesigns/device/stratix2/stratix2-index.jsp
- For eStore if you want to purchase devices:
  www.altera.com/buy/devices/buy-devices.html
- For OrCAD symbols:
  www.altera.com/support/software/download/pcb/pcb-pcb_index.html
- For Nios II 32-bit embedded processor solutions:
  www.altera.com/technology/embedded/emb-index.html

# 3. Software Installation

## Introduction

The instructions in this section explain how to install the following:

- DSP Development Kit CD-ROM
- Altera Complete Design Suite DVD
- MathWorks MATLAB/Simulink CD-ROM

## Requirements

Before starting the installation, verify that you have complied with the conditions described in "Software Requirements" on page 2–2.

## Installing the DSP Development Kit CD-ROM

The DSP Development Kit CD-ROM contains the following items:

- Reference designs for DSP application
- Design examples
- *Data Conversion HSMC Reference Manual*
- *Development Board Reference Manual* for Stratix III or Cyclone III development kit
- *DSP Development Kit Getting Started User Guide* (this document)
- Device data sheets and tutorials
- Schematic and board design files

To install the DSP Development Kit CD-ROM, perform the following steps:

1. Insert the DSP Development Kit CD-ROM into the CD-ROM drive.

   The CD-ROM should start an auto-install process. If it does not, browse to the CD-ROM drive and double-click on the **setup.exe** file.

2. Follow the on-screen instructions to complete the installation process.

   The installation program copies the DSP development kit files to the computer hard disk and creates a **Programs > Altera > DSP Development Kit** <*kit edition*> <*version#*> Windows Start menu shortcut. Use this shortcut to launch the development kit graphical user interface (GUI).

When the installation is complete, the DSP development kit installation program creates the directory structure example shown in Figure 3–1, where <*path*> is the DSP development kit installation directory.

Small differences exist within these directories depending on the actual kit contents and options.

**Figure 3–1.** DSP Development Kit Installed Directory Structure


Table 3–1 lists the file directory names and a description of their contents.

**Table 3–1.** Installed Directory Contents

| Directory Name | Description of Contents |
|---|---|
| **board_design_files** | Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design. |
| **demos** | Contains unsupported demonstration files for various use with the development board and/or HSMC. |
| **documents** | Contains the development kit documentation. |
| **examples** | Contains the sample design files for the DSP development kit. |
| **factory_recovery** | Contains programming files for use with the development kit board to return it to the factory default status. |

# Installing the Altera Complete Design Suite DVD

The Altera Complete Design Suite DVD contains the following items:

- Quartus II Software
- MegaCore IP Library
- Nios II Embedded Design Suite
- ModelSim-Altera Edition
- DSP Builder

The Quartus II software is the primary FPGA development tool used, along with the MATLAB software, to create the reference designs used in this development kit. Additionally, you may want to install the Nios II Embedded Design Suite. The Nios II embedded processor runs on Altera FPGAs. Some of the reference designs included in this development kit use the Nios II processor.

To install the Altera Complete Design Suite DVD, perform the following steps:

1. Insert the Altera Complete Design Suite DVD into the DVD drive.

2. On the startup screen, click **Install subscription package** for Stratix III and Stratix II DSP kits or click **Install free package** for Cyclone III DSP kit. Follow the on-screen instructions and accept all default settings.
3. Next, you can install the DSP Builder software by clicking the **Install** button for the software, which is located in the **Install additional software** section on the startup screen.

   ☞ If you plan to use the DSP Builder, install the MathWorks MATLAB and Simulink CD-ROM first. Also, because the MathWorks software trial licence is valid only for 30 days, only install the MathWorks MATLAB/Simulink CD-ROM when you are ready to use the DSP Builder, the Simulink software for DSP development, or the factory designs in Chapter 5, DSP Example Designs.

4. After installing the DSP Builder software, request and install a license to enable it. For information about obtaining a license file, refer to "Licensing Considerations" on page 3–4.

# Installing MathWorks MATLAB/Simulink CD-ROM

To install MathWorks software, perform the following steps:

1. Before installing, make sure that you have your Personal License Password (PLP) available. To obtain the 30-day evaluation license and for more information, visit MathWorks at www.mathworks.com.
2. If it is running, close the MATLAB/Simulink software.
3. Insert MathWorks MATLAB/Simulink CD-ROM. The MathWorks Installer automatically starts, displaying the **Welcome to The MathWorks Installer** dialog box.
4. In the dialog box, choose **Install** and click **Next**.
5. Enter your name, company name, and PLP in the **License Information** dialog box and click **Next**.
6. Review the software licensing agreement. If you agree with the terms, turn on **Yes** and click **Next**.
7. Select **Typical** or **Custom installation** (for any user-specific selections) and click **Next**.
8. Click **Install**.
9. Click **Finish**.

# Installing the USB-Blaster Driver

The series III DSP development boards include integrated USB-Blaster circuitry for FPGA programming. The series II development boards use an external USB-Blaster. However, for the host computer and development board to communicate, you must install the USB-Blaster driver on the host computer.

To download the USB-Blaster driver, go to the Altera support site at www.altera.com/support/software/drivers/dri-index.html. To install it, go to www.altera.com/support/software/drivers/usb-blaster/dri-usb-blaster-xp.html.

# Licensing Considerations

Before using the Quartus II software and the DSP Builder software, you must request a license file from the Altera website at www.altera.com/licensing and install it on your computer. When you request a license file, Altera emails you a **license.dat** file that enables the software.

To obtain a license, perform the following steps:

For the Stratix III and Stratix II DSP development kits, if you already have a Fixed PC or FloatNet Quartus II subscription, you can use that software instead of the Quartus II DKE software. However, you may still need to follow these instructions to obtain a license for the DSP Builder software if you do not already have one.

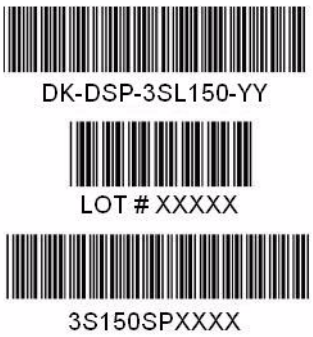
1. Go to the Altera website at www.altera.com/support/licensing/lic-choose.html.
2. Under **Development Kit Licenses Request**, click **Licenses for RoHS-Compliant Kits**.
3. Follow the on-screen instructions to request your license. You will receive a license file through email.
4. Before installing your license, close the following software if it is running on your computer:
   - Quartus II software
   - MAX+PLUS® II software
   - LeonardoSpectrum™ synthesis tool
   - Synplify software
   - ModelSim simulator
   - Precision RTL Synthesis software
5. To install your license, refer to the *Specifying the License File* section in the *Quartus II Installation & Licensing for Windows Manual*, which is included with the kit.

You will also receive a time-limited license for the DSP Builder software. This license is a perpetual license with free software upgrades for the first 180 days. After 180 days, you must purchase a renewal subscription for access to future software upgrades. For more information, refer to the Altera website at www.altera.com.

You need your NIC ID and the kit serial number to license the Quartus II software. Your NIC ID is a 12-character hexadecimal number that uniquely identifies your computer. You can find the NIC ID for your card by typing `ipconfig/all` at a command prompt. Your NIC ID is the number on the physical address line.

The kit serial number is an 11-digit code of the form 3S150SPXXXX where the Xs represent decimal numbers. This serial number is located on the development kit box. Refer to the serial number sticker in Figure 3–2. The serial number is the bottom-most number, which is 3S150SPXXXX in the example shown.

**Figure 3–2.** Serial Number Example



# 4. DSP Development Kit Hardware Setup

## Introduction

The instructions in this chapter explain how to power up your DSP development board and configure the FPGA with the appropriate supplied file.

## Requirements

Setting up your DSP development board requires the following software and hardware:

- Quartus II software installed on the host computer
- USB-Blaster driver software installed on the host computer

  The host computer, FPGA, and development board cannot communicate without the USB-Blaster driver software installed. For installation information, refer to "Installing the USB-Blaster Driver" on page 3–3.
- Data Conversion HSMC (Stratix III and Cyclone III development kits only)
- SLP-50 anti-aliasing filter
- SMA cable
- USB cable
- USB-Blaster (Stratix II development kit only)

## Powering Up the Board

Before powering up, prepare the board by performing the following steps:

1. Ensure that the POWER switch (Table 4–1) is in the OFF (or down) position.

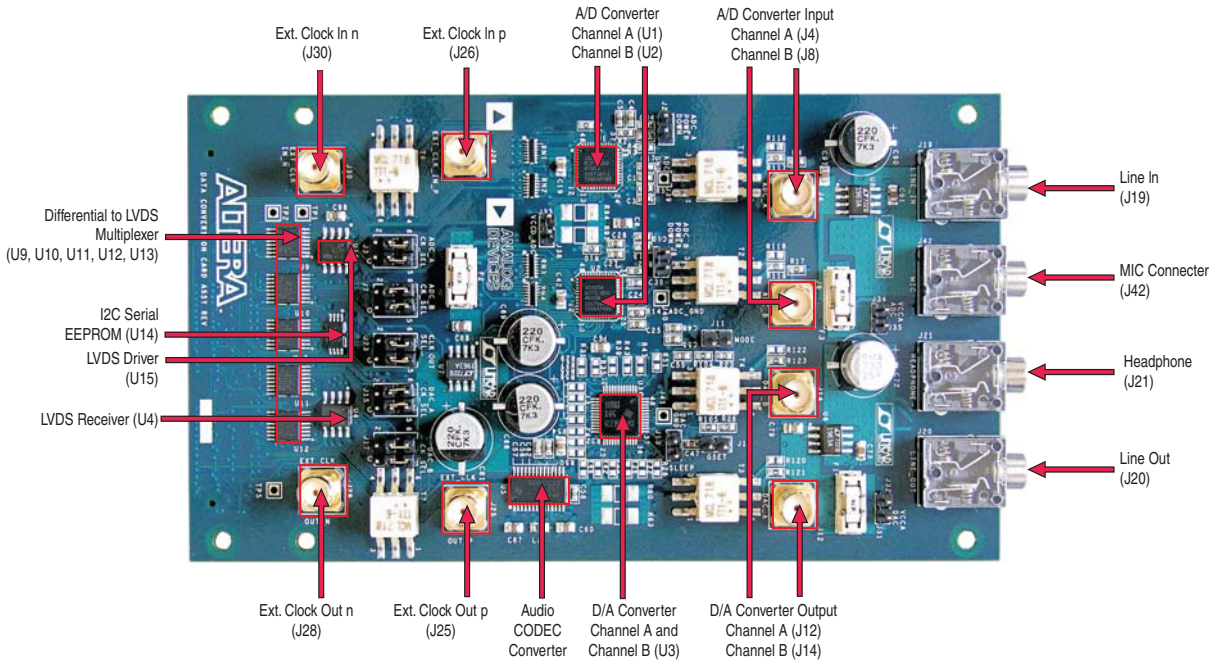
**Table 4–1.** Power Switches for DSP Boards

| Stratix III | Cyclone III | Stratix II |
|---|---|---|
| SW9 | SW2 | SW4 |

2. Ensure that the DIP switch and rotary switch settings are set correctly as described in Appendix A, Stratix III and Cyclone III Host Board Settings (for Cyclone III and Stratix III boards only).
3. Attach the Data Conversion HSMC to HSMC Port A on the left side of the development board (Cyclone III and Stratix III boards only). Verify the jumper configuration on the Data Conversion HSMC is set to the default settings provided in Appendix B, Data Conversion HSMC Jumper Settings.

   Figure 4–1 shows the Data Conversion HSMC that is used with the Stratix III and Cyclone III DSP development kits.

**Figure 4–1.** Data Conversion HSMC Card Layout and Components




Altera recommends that standoffs be installed in order to hold the two boards at the proper heights. The shorter standoffs should be installed in the four corners of the development board. Two of the longer standoffs should be installed in the mounting holes near the audio connectors on the Data Conversion HSMC. This arrangement minimizes the stress on the HSM connector.

Figure 4–2 and Figure 4–3 show the Data Conversion HSMC card connected to the Stratix III and Cyclone III development boards, respectively.

**Figure 4–2.** Data Conversion HSMC Card Connection to the Stratix III Development Board

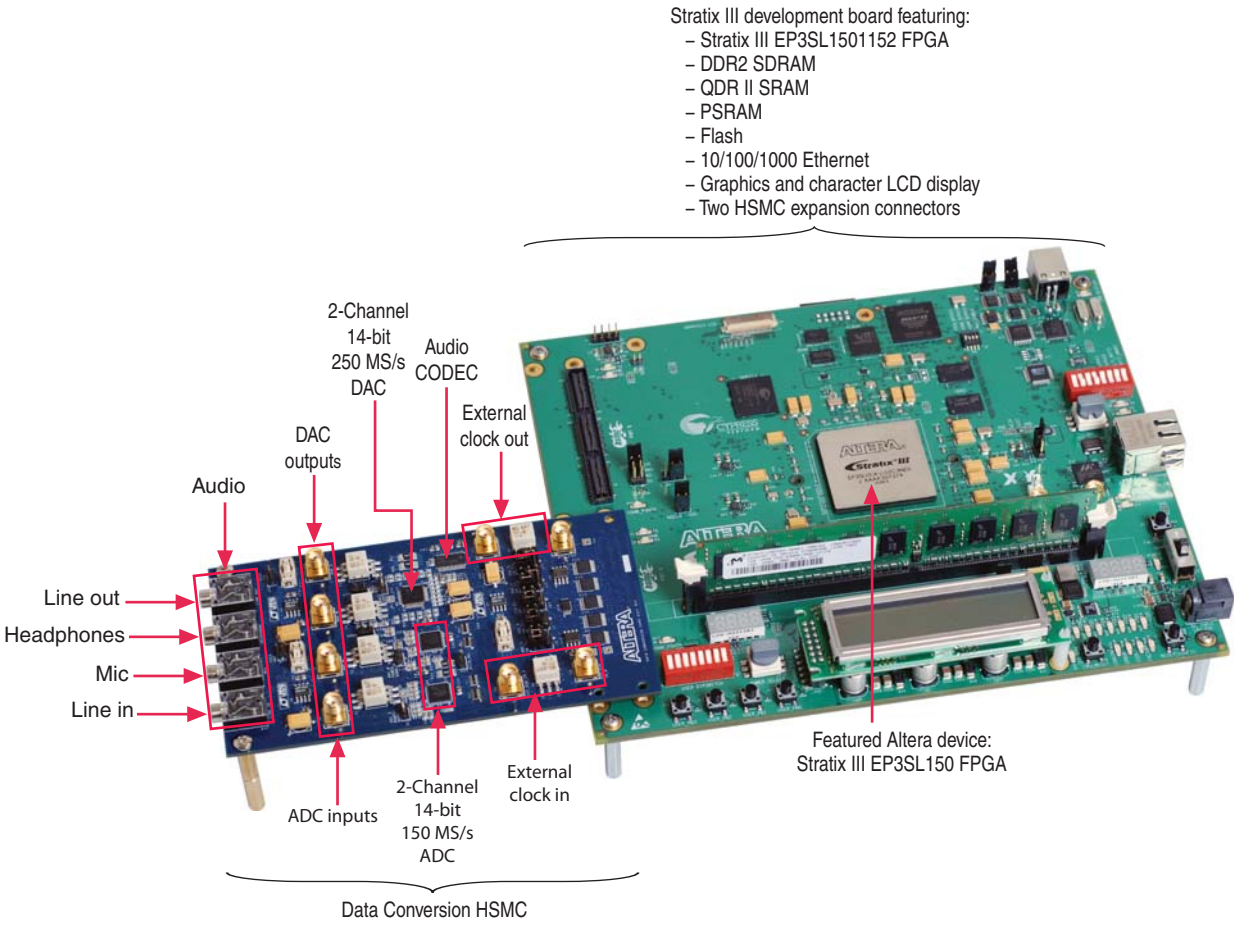
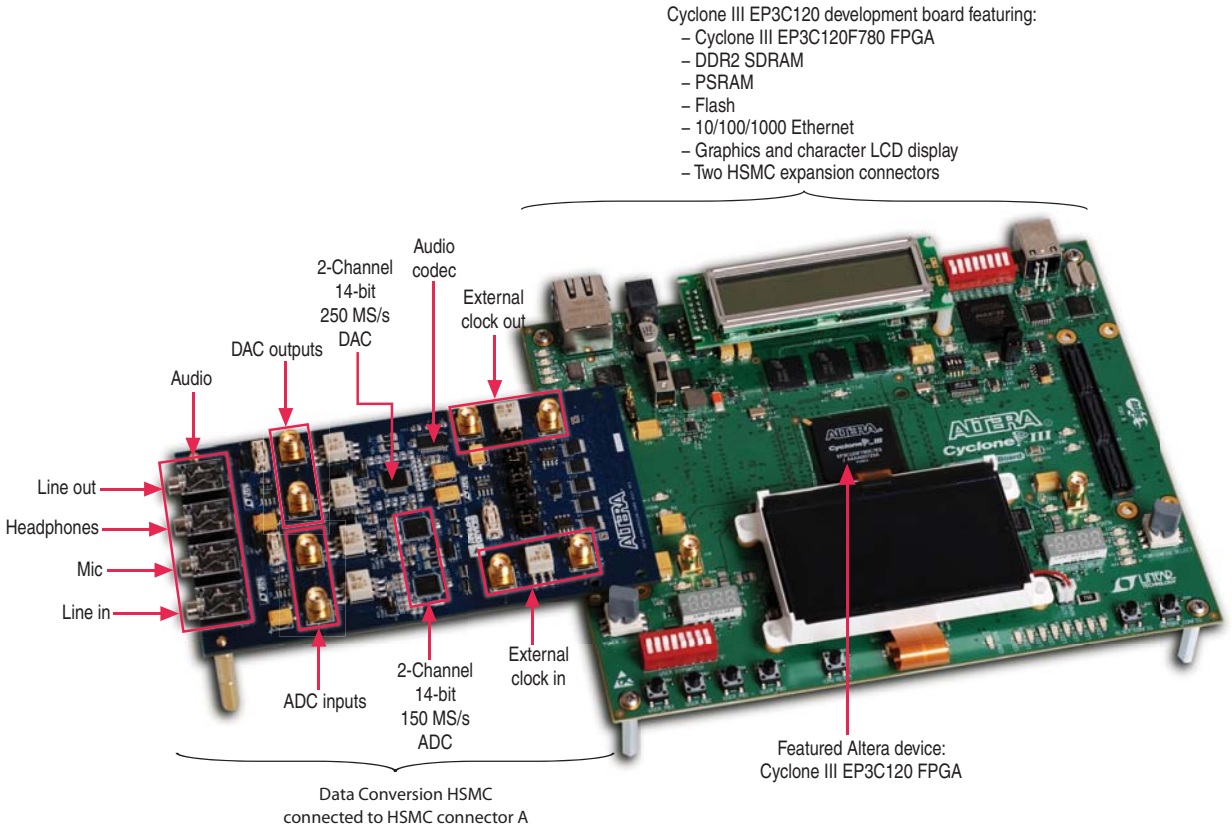


**Figure 4–3.** Data Conversion HSMC Card Connection to the Cyclone III Development Board




4. Attach the SLP-50 anti-aliasing filter to the ADC input (J1 for the Stratix II host boards, and J4 for the Data Conversion HSMC used with the Cyclone III and Stratix III DSP development kits).

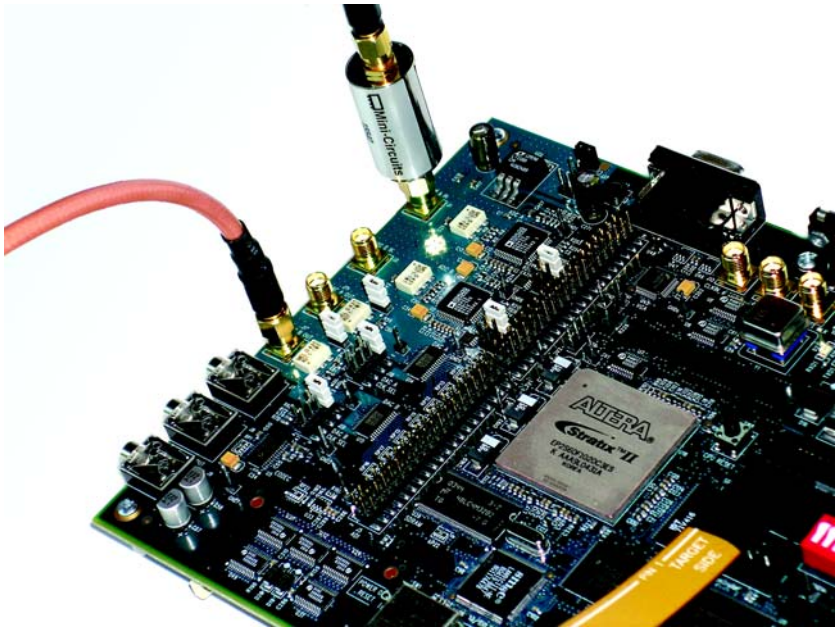
   The SLP-50 anti-aliasing filter from Mini-Circuits provides a 55-MHz cutoff frequency. Perform an external loopback from one of the D/A converters to one of the A/D converters by connecting the output of one to the input of the other, using the filter and cable assembly. If the cutoff frequency must be lower than 55 MHz, other filters may be used.

5. Attach the SMA cable to the DAC output (J17 for the Stratix II host boards, and J12 for the Data Conversion HSMC used with the Cyclone III and Stratix III DSP development kits).

6. Attach the other end of the SMA cable to the SLP-50 anti-aliasing filter.

   Figure 4–4 shows this connection for the Stratix II 2S60 DSP development board.

**Figure 4–4.** SMA Cable and SLP-50 Filter Installed



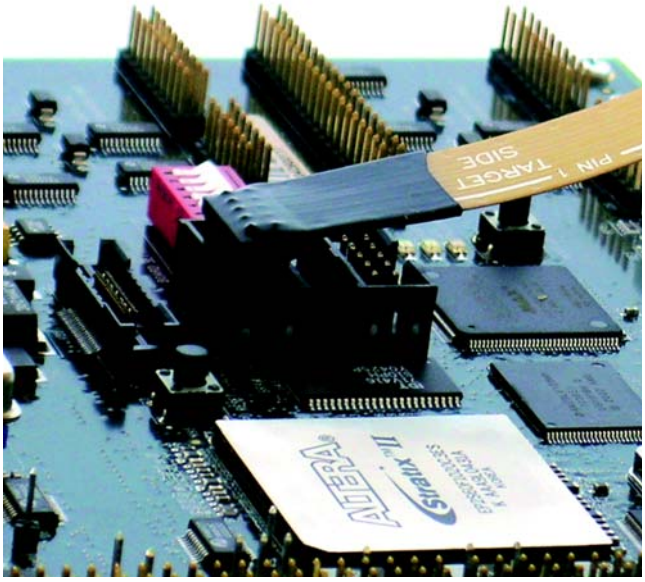

For the Stratix II-based boards, you must add additional jumpers for clocking. Follow the instructions in Appendix C, Clocking Jumpers for Stratix II Boards.

7. Enable USB-Blaster communications.

   Stratix III and Cyclone III DSP development kits have an integrated USB-Blaster on the host board. Simply connect the supplied USB cable to USB connector on the host board (J5 for Stratix III development board and J3 for Cyclone III development board).

   The Stratix II-based DSP development kits come with an external USB-Blaster. Connect the USB-Blaster cable's 10-pin female plug to the Stratix II device JTAG header on the development board (J21) and connect the USB cable to the USB-Blaster's connector. Connect the other end of the USB cable to your PC to configure the FPGA directly using an SRAM Object File (**.sof**). See Figure 4–5 for the USB-Blaster connections for the Stratix II board.

**Figure 4–5.** Connecting the USB_Blaster Cable to J21




8. Connect the power cable to the board and plug the other end into a power outlet, then turn on the board using the power-on switch shown in Figure 4–5.

After the board powers up, the on-board flash memory which ships pre-programmed with the factory design automatically configures the FPGA device. The CONF_DONE LED turns on, signifying that the FPGA is configured.

The factory design for each of the boards includes logic that makes some of the LEDs on the board display a "counting pattern."

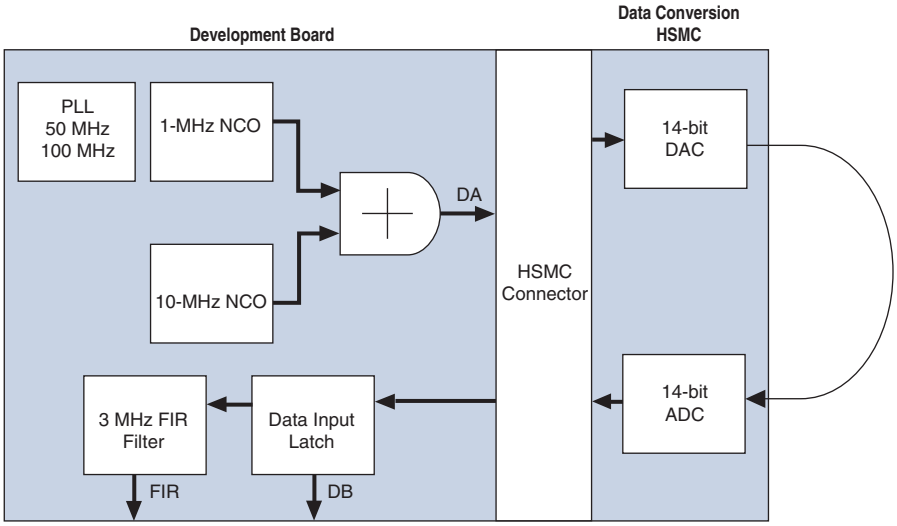
## Understanding the Factory Design

Factory Designs are provided for examining how FPGAs can be used for DSP applications. All of the provided designs are generally the same. A pair of sine waves are generated, one at 1 MHz and another at 10 MHz. These are added together and sent to a D/A converter. The resulting analog signal is looped back using a cable and filter to an A/D converter. The output is latched for examination and then fed to a 3-MHz FIR filter. The outputs of all of these stages are available for examination using the Altera SignalTap® II Logic Analyzer. The resolutions of the converters vary depending on the kit but the results are all very similar except for what can be expected from resolution changes.

The following design explains a specific design but the overall architecture is the same for all the kits.

Figure 5–1 shows a high-level view of the factory design and how it interacts with the D/A and A/D converters on the Data Conversion HSMC in the following sections.

**Figure 5–1.** Factory Design Functional Block Diagram *(Note 1)*




**Note to Figure 5–1:**

(1) The Stratix II DSP development kit has a 12-bit DAC and does not have an HSMC connector.

The design files for the factory design are installed from the DSP Development Kit CD-ROM in the directory: <*path*>**kits***<*specific kit*>**examples***<*specific kit*>**_dsp_example_ChA**. In the case of Stratix II DSP kit, the design files are in the <*FPGA designator*>**FactoryDesign** directory.

# Exercising the A/D and D/A Converter Performance Test

To test the A/D and D/A converter performance using the factory design, follow these steps:

1. "Configuring the Board"
2. "Collecting Data Using the SignalTap II Logic Analyzer" on page 5–3
3. "Analyzing Data in the MATLAB Software" on page 5–4

# Configuring the Board

The design you use to perform this tutorial exercise uses the Channel A DAC and the Channel A ADC portions of the board. To complete the circuit from end to end, install a link between the output of the Channel A DAC and the input to the Channel A ADC. For this link, use one of the SMA cables provided along with the SLP-50 filter.

To configure the board, perform the following steps:

Steps 1 and 2 apply to series III development kits only. For Stratix II development kit, connect as shown in Figure 4–4 on page 4–5.

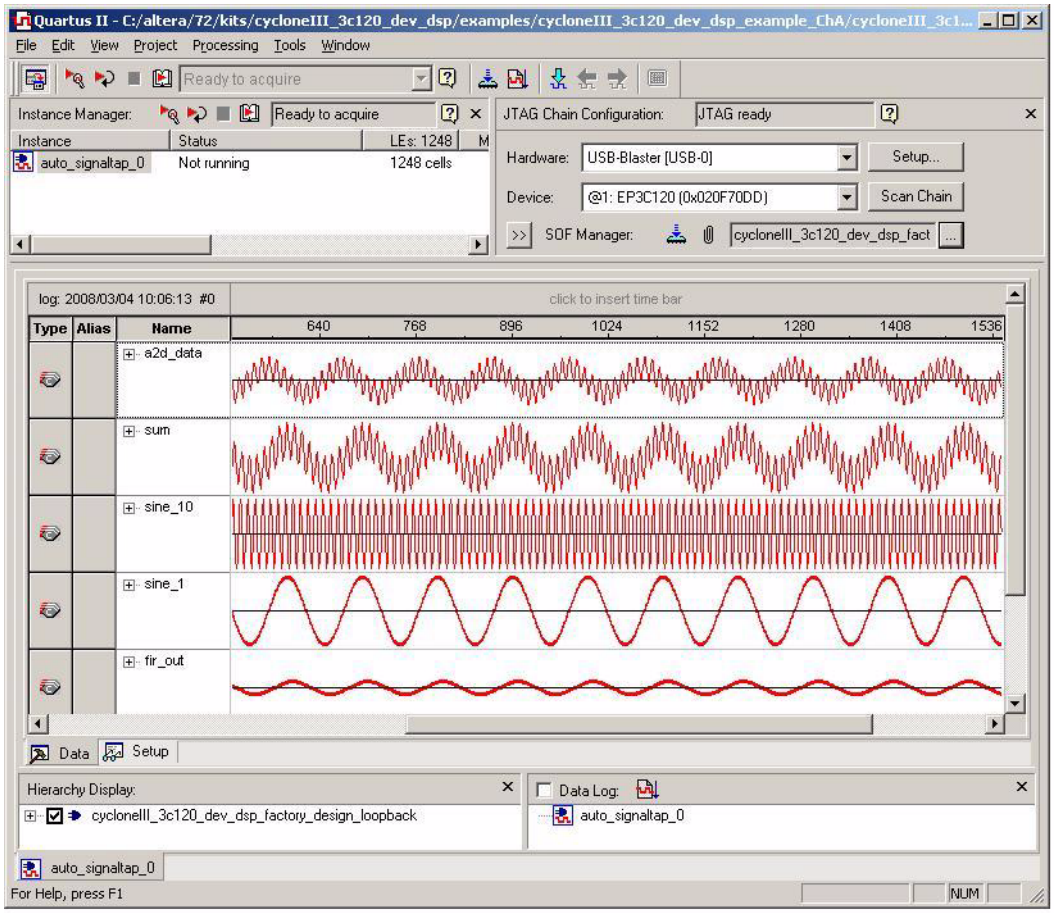
1. Attach the filter to the ADC input at J4.
2. Attach the SMA cable from the filter to the DAC output at J12. This connection is shown in Figure 5–1 on page 5–1.

   The clocks are jumpered and the system should now be powered up.
3. Start the Quartus II software and follow these steps:
   a. On the File menu, click **Open Project**.
   b. In the **Open Project** dialog box, browse to the appropriate directory:
   - For Stratix III DSP kit:
     <*path*>**\stratixIII_3sl150_dsp\ examples\ stratixIII_3sl150_dsp_example_ChA**
   - For Cyclone III DSP kit:
     <*path*>**\cycloneIII_3c120_dsp\examples\ cycloneIII_3c120_dsp_example_ChA**
   - For Stratix II DSP kit:
     <*path*>**\StratixII_DSP_Kit-**<*version*>**\Examples**<*kit type*>**\FactoryDesign**

   c. Select <*specific kit*>**_dsp_factory_design.qpf** (or **sines.qpf** for the Stratix II kit), which contains project definitions for reference design, and click **Open**.
   d. The SignalTap II file (**.stp**) provided with the design, **sines.stp**, is required also. On the File menu, click **Open**. Select **SignalTap II Logic Analyzer Files (*.stp)** from the **Files of type,** select **sines.stp**, and click **Open**.

      Figure 5–2 shows **sines.stp** displayed in the SignalTap II logic analyzer. You can click the "+" sign for the displayed waveform and observe the incoming data stream. Click the "-" sign to collapse the display after you are done so that the analysis shows correctly.

**Figure 5–2.** Sines.stp Displayed in the SignalTap II Logic Analyzer




If you modify and recompile the design, specify your new **.sof** and click **Program Device** in the SignalTap II window to configure the device with your **.sof**.

# Collecting Data Using the SignalTap II Logic Analyzer

To collect data from the design for analysis, perform the following steps:

1. Download the design in the FPGA using the Quartus II Programmer. In the SignalTap II window, click the **Program Device** icon to configure the FPGA.
2. In the **Instance Manager** section of the SignalTap II window, click **Run Analysis** and scroll through the window to observe the following:
   a. Observe the D/A converter output on `da[13..0]`. It shows the combination of the two sine waves, `sin_out[12..0]` and `sin10_out[12..0]`.
   b. Observe the A/D converter input of the signal looped back from the D/A on `db[13..0]`. It shows an attenuated combination of two sine waves.

   The A/D converter output is attenuated because of losses in the analog circuitry, transformers, and terminators on the board.

3. On the File menu, select **Create SignalTap II List File** and click **Create/Update**. The Quartus II software generates the file **sines_auto_signaltap_0.txt** in the project directory.

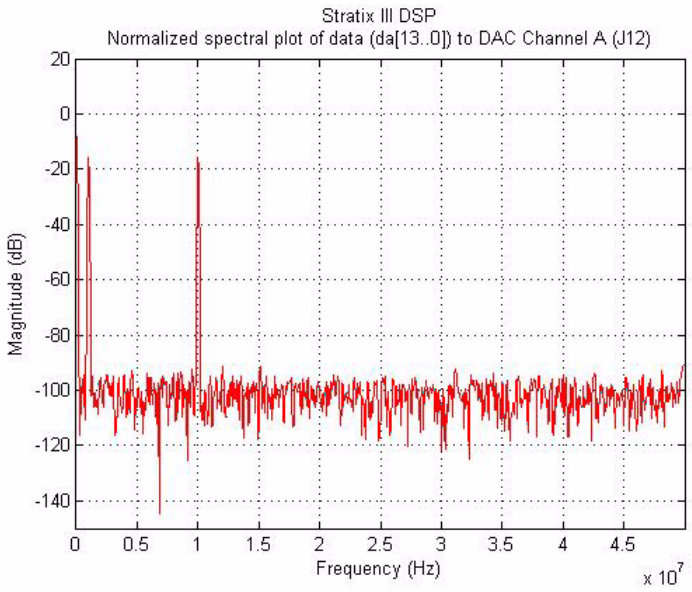
# Analyzing Data in the MATLAB Software

To analyze the spectrum content of the data from **sines_auto_signaltap_0.txt** in MATLAB, follow these steps:

1. First install and license MATLAB, which is provided in the MathWorks MATLAB/Simulink CD-ROM.
2. Start the MATLAB software.
3. Browse to the working directory.
4. To analyze the spectrum of the combined signal output to the D/A converter, perform the following steps:
   a. In the MATLAB command window, type the following command:
   `FIR_plot('sines_auto_signaltap_0.txt','a')` ↵
   b. The MATLAB software opens a display window, which shows a normalized plot of the DAC CHANNEL A output similar to that shown in Figure 5–3.

   Observe that the plotted graph of the peak spur level is below 80 db.

**Figure 5–3.** Normalized Spectral Plot of 14-bit Output to the Channel A D/A Converter



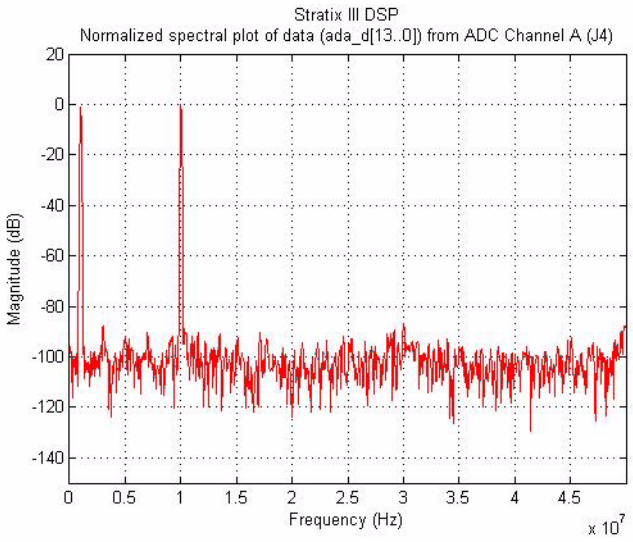
5. To analyze the spectrum of the combined signal through the system from the output to the D/A converter back to the input from the A/D converter, perform the following steps:

   a. In the MATLAB command window, type the following command:
   `FIR_plot('sines_auto_signaltap_0.txt','b')`↵

   b. The MATLAB software opens a display window, which shows a normalized plot of the ADC CHANNEL A input similar to that shown in Figure 5–4.

   The plot represents the resulting signal with all of the system noise and attenuation.

**Figure 5–4.** Normalized Spectral Plot of 14-bit ADC Channel A Output Data

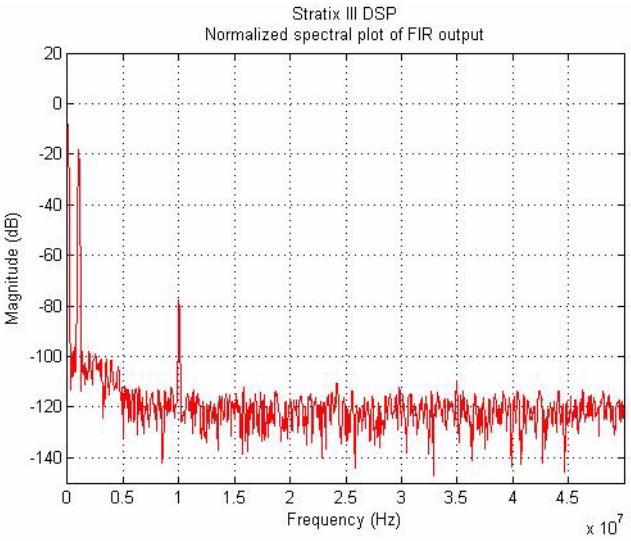



6. To analyze the final spectrum from the output of the 3-MHz FIR filter, in the MATLAB command window, type the following command:

   `FIR_plot('sines_auto_signaltap_0.txt','c')` ↵

   The MATLAB software opens a display window, which shows a normalized plot of the output of the 3-MHz FIR filter (Figure 5–5).

**Figure 5–5.** Normalized Spectral Plot of the Output Of the 3-MHz FIR Filter



# A. Stratix III and Cyclone III Host Board Settings

If your DSP board is based on the Stratix III or Cyclone III device, then ensure the switches and jumpers are set according to the following instructions:

1. The MAX II Control DIP Switch (SW2 for the Stratix III board and SW1 for the Cyclone III board) controls the PFL state among other things. Table A–1 shows the settings for this switch.

**Table A–1.** MAX II Control DIP Switch Settings (SW2 for Stratix III Board, SW1 for Cyclone III Board)

| Switch | Name | Function | | Default Position |
|---|---|---|---|---|
| | | Position 0 | Position 1 | |
| 1 | mW/mA | mW | mA | 0 |
| 2 | V/W | V | W | 1 |
| 3 | RSV0 | MAX_RESERVE0 | | X |
| 4 | RSV1 | MAX_RESERVE1 | | X |
| 5 | MAX0 | PFL Disable | PFL Enable | 1 |
| 6 | MAX1 | MAX_DIP1 | | X |
| 7 | MAX2 | MAX_DIP2 | | X |
| 8 | MAX3 | MAX_DIP3 | | X |

**Note to Table A–1:**

(1) X = don't care

2. Ensure that the Embedded-Blaster mini-DIP switch (SW1 for Stratix III board and SW3 for Cyclone III board) is set as shown in Table A–2.

**Table A–2.** Embedded-Blaster Mini-DIP Switch Settings (SW1 for Stratix III Board, SW3 for Cyclone III Board)

| Switch | Purpose | Setting |
|---|---|---|
| 1 | MAX II Enable | 1 |
| 2 | HSMC B Bypass | 0 |
| 3 | HSMC A Bypass | 0 |
| 4 | FPGA Bypass | 0 |

3. Ensure that the jumpers Device Select (J2 for Stratix III board, DEV_SEL – J6 for Cyclone III board) and JTAG Select (JTAG_SEL – J7 for Cyclone III and J3 for Stratix III) are both ON.
4. Ensure that the MSEL0 Jumper (J13) is ON (for Stratix III board only).
5. Verify that the PGM CONFIG SELECT rotary switch (SW3 for Stratix III board, SW5 for Cyclone III board) is set to 0.

   On power-up, the development board uses a preloaded configuration to demonstrate the board is operating correctly.

6. Set the User DIP switch (SW5 for Stratix III board and SW6 for Cyclone III board) as shown in Table A–3.

**Table A–3.** User DIP Switch Settings (SW5 for Stratix III Board, SW6 for Cyclone III Board)

| Switch | Setting |
|---|---|
| Stratix III (SW5) | Switch 2 closed; all other switches open. |
| Cyclone III (SW6) | All switches open. |

# B. Data Conversion HSMC Jumper Settings

If you are using the Stratix III or Cyclone III DSP boards with the Data Conversion HSMC, verify that the following jumper settings are made before using the DSP system.

- J2 ADC_A POWER DOWN removed
- J3 ADC_A CK SEL jumpers on pins 1-3 and 4-6
- J6 ADC_B POWER DOWN removed
- J7 ADC_B CK SEL jumpers on pins 1-3 and 4-6
- J10 DAC GSET removed
- J11 DAC MODE removed
- J13 DAC SLEEP removed
- J15 DAC_A CLK SEL jumpers on pins 1-3 and 4-6
- J17 DAC_B CLK SEL jumpers on pins 1-3 and 4-6
- J23 CLK OUT SEL jumpers on pins 1-3 and 2-4

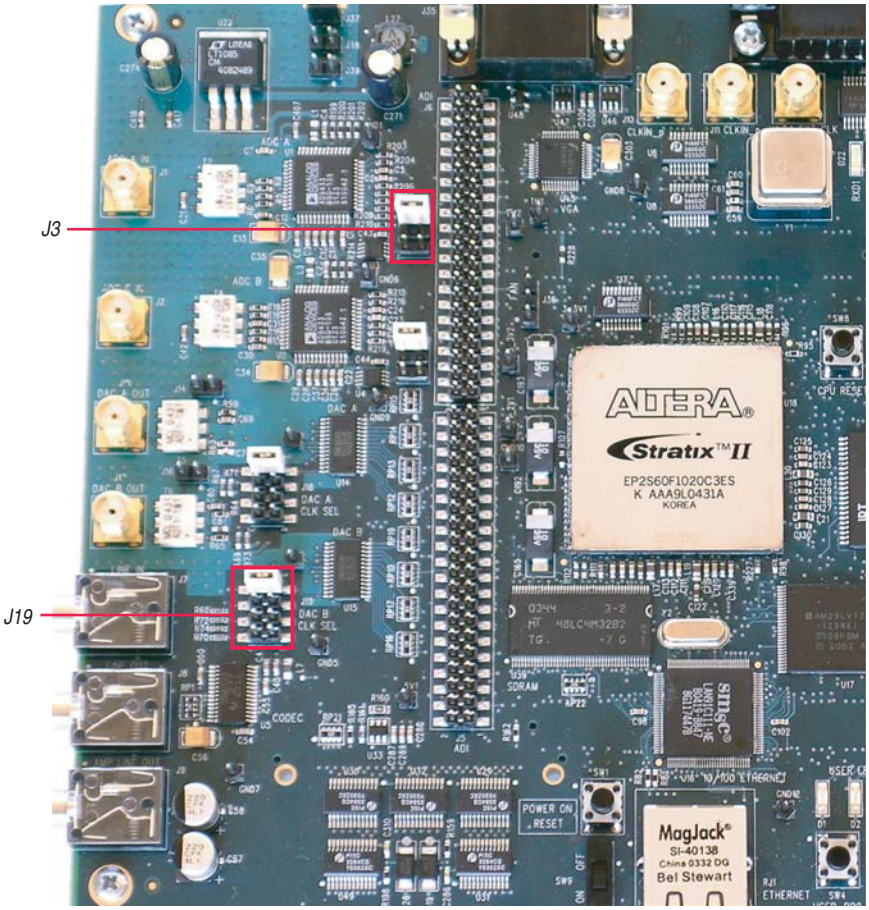
# C. Clocking Jumpers for Stratix II Boards

For Stratix II boards, verify the following jumpers, J3 and J19, are set correctly:

- For the ADC A clock, add a jumper to J3 between pins 1 and 2.
- For the DAC B clock, add a jumper to J19 between pins 1 and 2.

Figure C–1 shows the locations of J3 and J19.

**Figure C–1.** Locations of J3 and J19



## Revision History

The following table displays the revision history for this user guide.

| Date | Version | Changes Made |
|---|---|---|
| October 2008 | 1.0 | First publication |

## How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

| Contact *(Note 1)* | Contact Method | Address |
|---|---|---|
| Technical support | Website | www.altera.com/support |
| Technical training | Website | www.altera.com/training |
| | Email | custrain@altera.com |
| Altera literature services | Email | literature@altera.com |
| Non-technical support (General) | Email | nacomp@altera.com |
| (Software Licensing) | Email | authorization@altera.com |

**Note:**

(1) You can also contact your local Altera sales office or sales representative.

# Typographic Conventions

This document uses the typographic conventions shown in the following table.

| Visual Cue | Meaning |
|---|---|
| **Bold Type with Initial Capital Letters** | Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box. |
| **bold type** | Directory names, project names, disk drive names, file names, file name extensions, and software utility names are shown in bold type. Examples: **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file. |
| *Italic Type with Initial Capital Letters* | Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.* |
| *Italic type* | Internal timing parameters and variables are shown in italic type. Examples: $t_{PIA}$, $n + 1$.<br><br>Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file. |
| Initial Capital Letters | Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu. |
| "Subheading Title" | References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions." |
| `Courier type` | Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`.<br><br>Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier. |
| 1., 2., 3., and<br>a., b., c., etc. | Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
| ■ ■ | Bullets are used in a list of items when the sequence of the items is not important. |
| ✓ | The checkmark indicates a procedure that consists of one step only. |
|  | The hand points to information that requires special attention. |
|  | A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work. |
|  | A warning calls attention to a condition or possible situation that can cause injury to the user. |
| ↵ | The angled arrow indicates you should press the Enter key. |
|  | The feet direct you to more information on a particular topic. |